# XVME-9076
# Dual PMC Carrier Module
# for the XVME-6200

# USER'S MANUAL

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**8500-982C**

## 1. Functional Overview

The XMVE-9076 is a carrier board designed to provide two PMC expansion ports to an XVME-6200 series processor board. The carrier uses four lanes of PCI Express as its interface to the processor board, and uses an Intel bridge device to generate two independent channels of PCI-X. The XVME-9076 supports 3.3V, 133MHz signaling on each PMC site and can be configured for slower speeds including 33MHz PCI.

Onboard regulation provides 3.3V and 1.5V to the bridge chip and PMC sites. 5V signaling is not supported by this model and the board is keyed to 3.3V signaling only.

Key features of the XVME-9076 include:

- High-speed connection to the XVME-6200 processor board, using four lanes of PCI Express capable of 1GB/second bandwidth in each direction.
- Support for PMC cards at speeds up to 133Mhz.
- 3.3V-tolerant signaling using 64-bit PCI-X.
- Dual-channel PMC support for two PCM cards, each with its own bus resources.
- Seamless integration with an XVME-6200 processor board.

## 2. VLSI and Component Selection

Several considerations drove the selection of the bridge device needed to translate the PCI Express link from the processor board into the PCI-X interface required by the PMC sites. These include:

- Support for two channels of 64-bit PCI-X with dedicated bus resources for each channel
- Support for speeds up to 133MHz in dual-channel operation
- Source voltage less than or equal to the 5V supplied to the carrier board
- Sustainable production lifetime for 3 years or more
- Satisfaction of Xembedded environmental specifications

Several devices were studied, including components from NEC and Intel. Ultimately, the device selected was the Intel 41210 PCIe-to-PCIX Bridge. This device meets the above criteria and allows for dual-channel operation in a seamless operational mode. The Intel 41210 has additional features that lend itself well to the design of the XVME-9076:

- Configurable by an external microcontroller via SMBus.
- Efficient power consumption with a thermal profile suitable for in-stock heat sinks
- Selectable speed settings for debug assistance and end-user customization

## 3. Architectural Block Diagram

Figure 1 contains the functional block diagram of XVME-9090VR7 Remote I/O board.

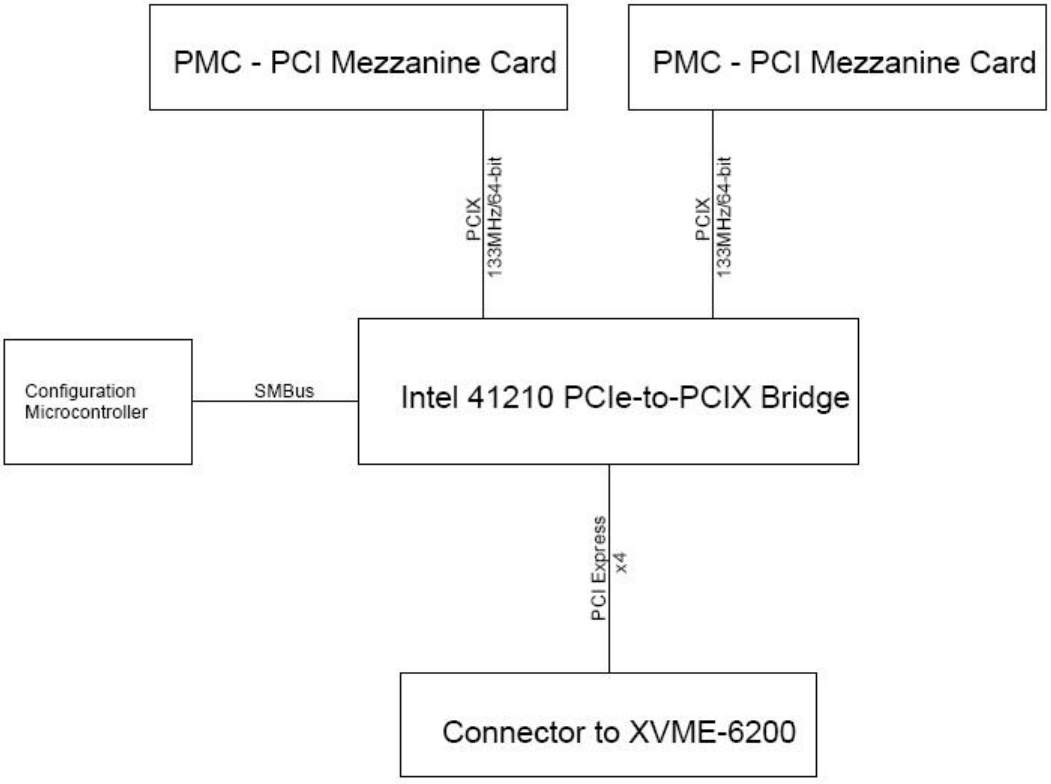



**Figure #1: Block Diagram**

## 4. Installing the XVME-9076 on an XVME-6200

The XVME-9076 adapter module connects directly to the XVME-6200 via P5 interconnect connector. Additional hardware (supplied with the XVME-9076) needs to be mounted to the boards.

- Three or Four corner standoffs (four are supplied. Some older XVME-6200's can only be connected in three corners).
- Three to four pairs of standoff screws (four parts are supplied. Some older XVME-6200's can only be connected in three corners).

The XVME-9076 and the XVME-6200 are shipped separately and are assembled by the integrator.

NOTE: The XVME-9076 and the XVME-6200 will be damaged if the XVME-6200 and the XVME-9076 are not fasten together BEFORE inserting into the VMEbus chassis. AT NO TIME should these two modules be inserted without being fasten together. Damage will not be covered under warranty.

## 4.1 Installing the XVME-9076 to the host XVME-6200Processor Module.

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME-6200processor module.
4. Remove the XVME-6200from the VME backplane, as follows:
• Gently pull on the face plate until it slides out of the chassis

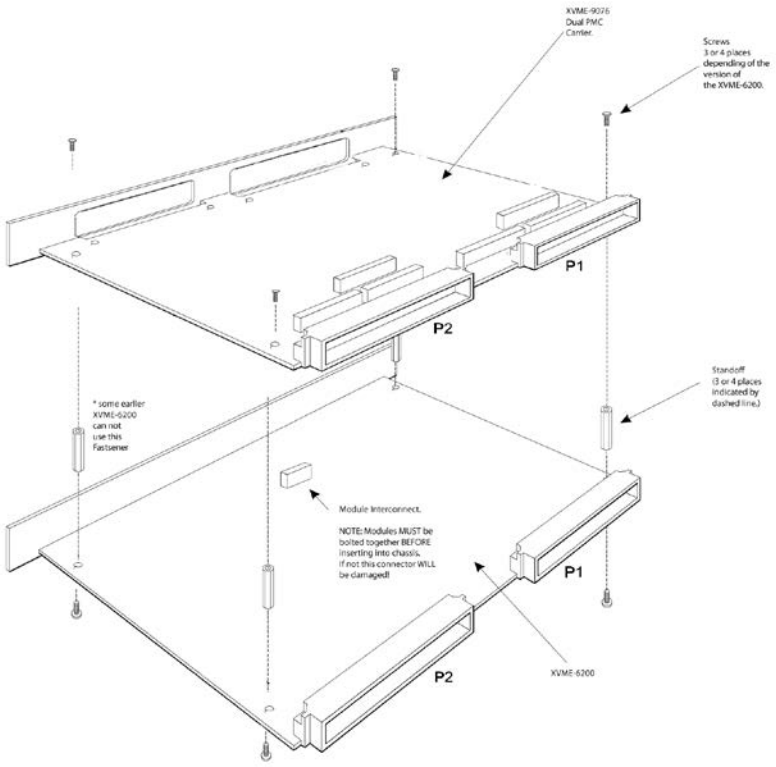



Figure 4-1 Installing XVME-9076 to the XVME-6200

5. Place the XVME-6200 on a static-free surface with the P6 connector facing up.
6. Align the P5 connector on the XVME-9076 with the same connectors on the XVME-6200.
7. Gently press the two boards together. Do not bend or twist the XVME-9076.
8. Add standoffs (4) and standoff screws (4 pairs) as illustrated in Figure 4-1. Continue to use care not to bend or twist the modules while assembling them.
9. Clear two adjacent card cage slots.
10. Align the two connected modules (with the XVME-9076 on the right) on the card guides in the slots.
11. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
12. Tighten the screws on the front panel of the XVME-6200 processor module and the XVME-9076 module to secure the connected modules into place. The installation is complete.

## 5. Interconnect Definition

The XVME-9076 supports the following interconnects to the processor board and the PMC sites.

| Connector | Function |
|---|---|
| VME P1 connector to backplane | Supplies power and required VME loopbacks |
| VME P2 connector to backplane | Supplies power and PMC I/O to PMC site 1 |
| VME P4 connector to backplane (typically called out as P0 on VME boards and optional) | Supplies PMC I/O to PMC site 2 |
| PCIe P5 connector to processor board | Supplies PCIe interface between the XVME-9076 and the processor board |
| J11-J14 PMC connectors | Supplies PMC connectors to PMC site 1 |
| J21-J24 PMC connectors | Supplies PMC connectors to PMC site 2 |

### 5.1 P1 Pin Definitions

| Pin Number | Signal | Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|---|---|
| A1 | NC | B1 | NC | C1 | NC |
| A2 | NC | B2 | NC | C2 | NC |
| A3 | NC | B3 | NC | C3 | NC |
| A4 | NC | B4 | VME_BG_ IN_OUT0# | C4 | NC |
| A5 | NC | B5 | | C5 | NC |
| A6 | NC | B6 | VME_BG_ IN_OUT1# | C6 | NC |
| A7 | NC | B7 | | C7 | NC |
| A8 | NC | B8 | VME_BG_ IN_OUT2# | C8 | NC |
| A9 | GND | B9 | | C9 | GND |
| A10 | NC | B10 | VME_BG_ IN_OUT3# | C10 | NC |
| A11 | GND | B11 | | C11 | NC |
| A12 | NC | B12 | NC | C12 | NC |
| A13 | NC | B13 | NC | C13 | NC |
| A14 | NC | B14 | NC | C14 | NC |
| A15 | GND | B15 | NC | C15 | NC |
| A16 | NC | B16 | NC | C16 | NC |
| A17 | GND | B17 | NC | C17 | NC |
| A18 | NC | B18 | NC | C18 | NC |
| A19 | GND | B19 | NC | C19 | NC |
| A20 | NC | B20 | GND | C20 | NC |
| A21 | VME_IACK_ IN_OUT# | B21 | NC | C21 | NC |
| A22 | | B22 | NC | C22 | NC |
| A23 | NC | B23 | GND | C23 | NC |
| A24 | NC | B24 | NC | C24 | NC |
| A25 | NC | B25 | NC | C25 | NC |
| A26 | NC | B26 | NC | C26 | NC |
| A27 | NC | B27 | NC | C27 | NC |
| A28 | NC | B28 | NC | C28 | NC |

| | | | | | |
|---|---|---|---|---|---|
| A29 | NC | B29 | NC | C29 | NC |
| A30 | NC | B30 | NC | C30 | NC |
| A31 | -12V | B31 | NC | C31 | +12V |
| A32 | +5V | B32 | +5V | C32 | +5V |

Note: Power signals are called out in red.

## 5.2 P2 Pin Definitions

| Pin Number | Signal | Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|---|---|
| A1 | PMC1_IO2 | B1 | +5V | C1 | PMC1_IO1 |
| A2 | PMC1_IO4 | B2 | GND | C2 | PMC1_IO3 |
| A3 | PMC1_IO6 | B3 | NC | C3 | PMC1_IO5 |
| A4 | PMC1_IO8 | B4 | NC | C4 | PMC1_IO7 |
| A5 | PMC1_IO10 | B5 | NC | C5 | PMC1_IO9 |
| A6 | PMC1_IO12 | B6 | NC | C6 | PMC1_IO11 |
| A7 | PMC1_IO14 | B7 | NC | C7 | PMC1_IO13 |
| A8 | PMC1_IO16 | B8 | NC | C8 | PMC1_IO15 |
| A9 | PMC1_IO18 | B9 | NC | C9 | PMC1_IO17 |
| A10 | PMC1_IO20 | B10 | NC | C10 | PMC1_IO19 |
| A11 | PMC1_IO22 | B11 | NC | C11 | PMC1_IO21 |
| A12 | PMC1_IO24 | B12 | GND | C12 | PMC1_IO23 |
| A13 | PMC1_IO26 | B13 | +5V | C13 | PMC1_IO25 |
| A14 | PMC1_IO28 | B14 | NC | C14 | PMC1_IO27 |
| A15 | PMC1_IO30 | B15 | NC | C15 | PMC1_IO29 |
| A16 | PMC1_IO32 | B16 | NC | C16 | PMC1_IO31 |
| A17 | PMC1_IO34 | B17 | NC | C17 | PMC1_IO33 |
| A18 | PMC1_IO36 | B18 | NC | C18 | PMC1_IO35 |
| A19 | PMC1_IO38 | B19 | NC | C19 | PMC1_IO37 |
| A20 | PMC1_IO40 | B20 | NC | C20 | PMC1_IO39 |
| A21 | PMC1_IO42 | B21 | NC | C21 | PMC1_IO41 |
| A22 | PMC1_IO44 | B22 | GND | C22 | PMC1_IO43 |
| A23 | PMC1_IO46 | B23 | NC | C23 | PMC1_IO45 |
| A24 | PMC1_IO48 | B24 | NC | C24 | PMC1_IO47 |
| A25 | PMC1_IO50 | B25 | NC | C25 | PMC1_IO49 |
| A26 | PMC1_IO52 | B26 | NC | C26 | PMC1_IO51 |
| A27 | PMC1_IO54 | B27 | NC | C27 | PMC1_IO53 |
| A28 | PMC1_IO56 | B28 | NC | C28 | PMC1_IO55 |
| A29 | PMC1_IO58 | B29 | NC | C29 | PMC1_IO57 |
| A30 | PMC1_IO60 | B30 | NC | C30 | PMC1_IO59 |
| A31 | PMC1_IO62 | B31 | GND | C31 | PMC1_IO61 |
| A32 | PMC1_IO64 | B32 | +5V | C32 | PMC1_IO63 |

Note: Power signals are called out in red.

## 5.3 P4 (P0) Pin Definitions

| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| A1 | NC | B1 | NC | C1 | NC |
| A2 | NC | B2 | NC | C2 | GND |
| A3 | NC | B3 | NC | C3 | GND |
| A4 | NC | B4 | NC | C4 | GND |
| A5 | NC | B5 | NC | C5 | GND |
| A6 | NC | B6 | NC | C6 | NC |
| A7 | PMC2_I0-5 | B7 | PMC2_I0-4 | C7 | PMC2_I0-3 |
| A8 | PMC2_I0-10 | B8 | PMC2_I0-9 | C8 | PMC2_I0-8 |
| A9 | PMC2_I0-15 | B9 | PMC2_I0-14 | C9 | PMC2_I0-13 |
| A10 | PMC2_I0-20 | B10 | PMC2_I0-19 | C10 | PMC2_I0-18 |
| A11 | PMC2_I0-25 | B11 | PMC2_I0-24 | C11 | PMC2_I0-23 |
| A12 | PMC2_I0-30 | B12 | PMC2_I0-29 | C12 | PMC2_I0-28 |
| A13 | PMC2_I0-35 | B13 | PMC2_I0-34 | C13 | PMC2_I0-33 |
| A14 | PMC2_I0-40 | B14 | PMC2_I0-39 | C14 | PMC2_I0-38 |
| A15 | PMC2_I0-45 | B15 | PMC2_I0-44 | C15 | PMC2_I0-43 |
| A16 | PMC2_I0-50 | B16 | PMC2_I0-49 | C16 | PMC2_I0-48 |
| A17 | PMC2_I0-55 | B17 | PMC2_I0-54 | C17 | PMC2_I0-53 |
| A18 | PMC2_I0-60 | B18 | PMC2_I0-59 | C18 | PMC2_I0-58 |
| A19 | NC | B19 | PMC2_I0-64 | C19 | PMC2_I0-63 |
| | | | | | |
| Pin | Signal | Pin | Signal | Pin | Signal |
| D1 | NC | E1 | NC | F1 | GND |
| D2 | NC | E2 | NC | F2 | GND |
| D3 | NC | E3 | NC | F3 | GND |
| D4 | NC | E4 | NC | F4 | GND |
| D5 | NC | E5 | NC | F5 | GND |
| D6 | NC | E6 | NC | F6 | GND |
| D7 | PMC2_I0-2 | E7 | PMC2_I0-1 | F7 | GND |
| D8 | PMC2_I0-7 | E8 | PMC2_I0-6 | F8 | GND |
| D9 | PMC2_I0-12 | E9 | PMC2_I0-11 | F9 | GND |
| D10 | PMC2_I0-17 | E10 | PMC2_I0-16 | F10 | GND |
| D11 | PMC2_I0-22 | E11 | PMC2_I0-21 | F11 | GND |
| D12 | PMC2_I0-27 | E12 | PMC2_I0-26 | F12 | GND |
| D13 | PMC2_I0-32 | E13 | PMC2_I0-31 | F13 | GND |
| D14 | PMC2_I0-37 | E14 | PMC2_I0-36 | F14 | GND |
| D15 | PMC2_I0-42 | E15 | PMC2_I0-41 | F15 | GND |
| D16 | PMC2_I0-47 | E16 | PMC2_I0-46 | F16 | GND |
| D17 | PMC2_I0-52 | E17 | PMC2_I0-51 | F17 | GND |
| D18 | PMC2_I0-57 | E18 | PMC2_I0-56 | F18 | GND |
| D19 | PMC2_I0-62 | E19 | PMC2_I0-61 | F19 | GND |

Note: Power signals are called out in red.

## 5.4 P5 Pin Definitions

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | PCIE_XMT_LN0_DN | 4 | PCIE_RCV_LN0_DN |
| 5 | PCIE_XMT_LN0_DP | 6 | PCIE_RCV_LN0_DP |
| 7 | GND | 8 | GND |
| 9 | PCIE_XMT_LN1_DN | 10 | PCIE_RCV_LN1_DN |
| 11 | PCIE_XMT_LN1_DP | 12 | PCIE_RCV_LN1_DP |
| 13 | GND | 14 | GND |
| 15 | PCIE_XMT_LN2_DN | 16 | PCIE_RCV_LN2_DN |
| 17 | PCIE_XMT_LN2_DP | 18 | PCIE_RCV_LN2_DP |
| 19 | GND | 20 | GND |
| 21 | PCIE_XMT_LN3_DN | 22 | PCIE_RCV_LN3_DN |
| 23 | PCIE_XMT_LN3_DP | 24 | PCIE_RCV_LN3_DP |
| 25 | GND | 26 | GND |
| 27 | GND | 28 | GND |
| 29 | GND | 30 | GND |
| 31 | GND | 32 | GND |
| 33 | CK_100M_PCIE_DP | 34 | GND |
| 35 | CK_100M_PCIE_DN | 36 | RST_PCIE# |
| 37 | GND | 38 | GND |
| 39 | GND | 40 | GND |
| 41 | GND | 42 | GND |
| 43 | GND | | |

## 5.5 J11-J24 Pin Definitions

J11, J21

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | TCK | 2 | -12V |
| 3 | GND | 4 | INTA* |
| 5 | INTB* | 6 | INTC* |
| 7 | BUSMODE1* | 8 | +5V |
| 9 | INTD* | 10 | PCI-RSVD14B |
| 11 | GND | 12 | PCI-RSVD |
| 13 | CLK | 14 | GND |
| 15 | GND | 16 | GNT* |
| 17 | REQ* | 18 | +5V |
| 19 | V_I/O | 20 | PAD(31) |
| 21 | PAD(28) | 22 | PAD(27) |
| 23 | PAD(25) | 24 | GND |
| 25 | GND | 26 | C_BE3* |
| 27 | PAD(22) | 28 | PAD(21) |
| 29 | PAD(19) | 30 | +5V |
| 31 | V_I/O | 32 | PAD(17) |
| 33 | FRAME* | 34 | GND |

| | | | |
|---|---|---|---|
| 35 | GND | 36 | IRDY* |
| 37 | DEVSEL* | 38 | +5V |
| 39 | GND | 40 | PLOCK* |
| 41 | SDONE | 42 | SBO |
| 43 | PAR | 44 | GND |
| 45 | V_I/O | 46 | PAD(15) |
| 47 | PAD(12) | 48 | PAD(11) |
| 49 | PAD(9) | 50 | +5V |
| 51 | GND | 52 | C_BE0* |
| 53 | PAD(6) | 54 | PAD(5) |
| 55 | PAD(4) | 56 | GND |
| 57 | V_I/O | 58 | PAD(3) |
| 59 | PAD(2) | 60 | PAD(1) |
| 61 | PAD(0) | 62 | +5V |
| 63 | GND | 64 | REQ64* |

J12, J22

| Pin Number | Name | Pin Number | Name |
|---|---|---|---|
| 1 | +12V | 2 | TRST* |
| 3 | TMS | 4 | TDO |
| 5 | TDI | 6 | GND |
| 7 | GND | 8 | PCI-RSVD* |
| 9 | PCI-RSVD* | 10 | PCI-RSVD* |
| 11 | BUSMODE2* | 12 | +3.3V |
| 13 | RST* | 14 | BUSMODE3* |
| 15 | +.3V | 16 | BUSMODE4* |
| 17 | PCI-RSVD* | 18 | GND |
| 19 | PAD(30) | 20 | PAD(29) |
| 21 | GND | 22 | PAD(26) |
| 23 | PAD(24) | 24 | +3.3V |
| 25 | IDSEL | 26 | PAD(23) |
| 27 | +3.3V | 28 | pad(20) |
| 29 | PAD(18) | 30 | GND |
| 31 | PAD(16) | 32 | C_BD2* |
| 33 | GND | 34 | PMC-RSVD |
| 35 | TRDY* | 36 | +3.3V |
| 37 | GND | 38 | STOP* |
| 39 | PERR* | 40 | GND |
| 41 | +3.3V | 42 | SERR* |
| 43 | C_BD1* | 44 | GND |
| 45 | PAD(14) | 46 | PAD(13) |
| 47 | GND | 48 | PAD(10) |
| 49 | PAD(8) | 50 | +3.3V |
| 51 | PAD(7) | 52 | PMC-RSVD |
| 53 | +3.3V | 54 | PMC-RSVD |
| 55 | PMC-RSVD | 56 | GND |
| 57 | PMC-RSVD | 58 | PMC-RSVD |
| 59 | GND | 60 | PMC-RSVD |
| 61 | ACK64* | 62 | +3.3V |
| 63 | GND | 64 | PMC-RSVD |

J13/J23

| Pin Number | Name | Pin Number | Name |
|---|---|---|---|
| 1 | NC | 2 | GND |
| 3 | GND | 4 | C/BE7# |
| 5 | C/BE6# | 6 | C/BE5# |
| 7 | C/BE4# | 8 | GND |
| 9 | +3.3V | 10 | PAR64 |
| 11 | PAD(63) | 12 | PAD(62) |
| 13 | PAD(61) | 14 | GND |
| 15 | GND | 16 | PAD(60) |
| 17 | PAD(59) | 18 | PAD(58) |
| 19 | PAD(57) | 20 | GND |
| 21 | +3.3V | 22 | PAD(56) |
| 23 | PAD(55) | 24 | PAD(54) |
| 25 | PAD(53) | 26 | GND |
| 27 | GND | 28 | PAD(52) |
| 29 | PAD(51) | 30 | PAD(50) |
| 31 | PAD(49) | 32 | GND |
| 33 | GND | 34 | PAD(48) |
| 35 | PAD(47) | 36 | PAD(46) |
| 37 | PAD(45) | 38 | GND |
| 39 | +3.3V | 40 | PAD(44) |
| 41 | PAD(43) | 42 | PAD(42) |
| 43 | PAD(41) | 44 | GND |
| 45 | GND | 46 | PAD(40) |
| 47 | PAD(39) | 48 | PAD(38) |
| 49 | PAD(37) | 50 | GND |
| 51 | GND | 52 | PAD(36) |
| 53 | PAD(35) | 54 | PAD(34) |
| 55 | PAD(33) | 56 | GND |
| 57 | +3.3V | 58 | PAD(32) |
| 59 | NC | 60 | NC |
| 61 | NC | 62 | GND |
| 63 | GND | 64 | NC |

J14/J24

| Pin Number | Name | Pin Number | Name |
|---|---|---|---|
| 1 | USER I/O - 1 | 2 | USER I/O - 2 |
| 3 | USER I/O - 3 | 4 | USER I/O - 4 |
| 5 | USER I/O - 5 | 6 | USER I/O - 6 |
| 7 | USER I/O - 7 | 8 | USER I/O - 8 |
| 9 | USER I/O - 9 | 10 | USER I/O - 10 |
| 11 | USER I/O - 11 | 12 | USER I/O - 12 |
| 13 | USER I/O - 13 | 14 | USER I/O - 14 |
| 15 | USER I/O - 15 | 16 | USER I/O - 16 |
| 17 | USER I/O - 17 | 18 | USER I/O - 18 |
| 19 | USER I/O - 19 | 20 | USER I/O - 20 |
| 21 | USER I/O - 21 | 22 | USER I/O - 22 |
| 23 | USER I/O - 23 | 24 | USER I/O - 24 |
| 25 | USER I/O - 25 | 26 | USER I/O - 26 |

| | | | |
|---|---|---|---|
| 27 | USER I/O - 27 | 28 | USER I/O - 28 |
| 29 | USER I/O - 29 | 30 | USER I/O - 30 |
| 31 | USER I/O - 31 | 32 | USER I/O - 32 |
| 33 | USER I/O - 33 | 34 | USER I/O - 34 |
| 35 | USER I/O - 35 | 36 | USER I/O - 36 |
| 37 | USER I/O - 37 | 38 | USER I/O - 38 |
| 39 | USER I/O - 39 | 40 | USER I/O - 40 |
| 41 | USER I/O - 41 | 42 | USER I/O - 42 |
| 43 | USER I/O - 43 | 44 | USER I/O - 44 |
| 45 | USER I/O - 45 | 46 | USER I/O - 46 |
| 47 | USER I/O - 47 | 48 | USER I/O - 48 |
| 49 | USER I/O - 49 | 50 | USER I/O - 50 |
| 51 | USER I/O - 51 | 52 | USER I/O - 52 |
| 53 | USER I/O - 53 | 54 | USER I/O - 54 |
| 55 | USER I/O - 55 | 56 | USER I/O - 56 |
| 57 | USER I/O - 57 | 58 | USER I/O - 58 |
| 59 | USER I/O - 59 | 60 | USER I/O - 60 |
| 61 | USER I/O - 61 | 62 | USER I/O - 62 |
| 63 | USER I/O - 63 | 64 | USER I/O - 64 |

# 6. Functional Configuration Options

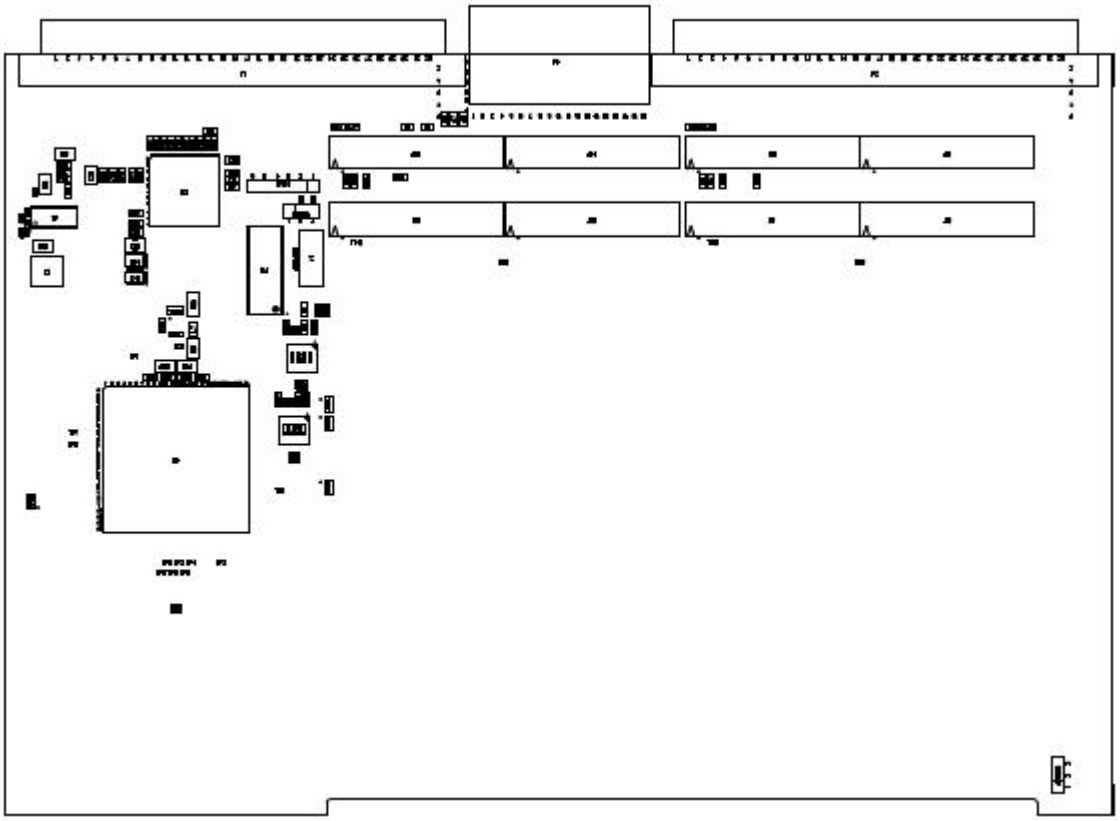
## 6.1 Jumpers

The following table Lists XVME-9090 jumpers, their default positions, and their functions.

| Jumper | Position | Function |
|---|---|---|
| ORBGND | Not populated ✓ | Chassis ground isolated from digital ground |
| | Pins 1-2 | Chassis ground isolated from digital ground |
| | Pins 2-3 | Chassis ground isolated tied to digital ground |
| CONFIG | Not populated ✓ | Use 41210 default values at startup |
| | Pins 1-2 | Use 41210 default values at startup |
| | Pins 2-3 | Load 41210 configuration data from µcontroller |

✓ denotes default

COMPONENT SIDE VIEW



## 6.2 Switches

SW1 on the XVME-9076 is a 4 position DIP switch used to manually assign SMBus addresses for the Intel 41210 Bridge device.

| Position | Open | Closed |
|---|---|---|
| 1 | SMBus 1 set to 3.3V | SMBus 1 set to 0V |
| 2 | SMBus 2 set to 3.3V | SMBus 2 set to 0V |
| 3 | SMBus 3 set to 3.3V | SMBus 3 set to 0V |
| 4 | SMBus 5 set to 3.3V | SMBus 5 set to 0V |

SW2 and SW3 on the XVME-9076 are 4 position DIP switches used to control the bus speed on PMC site 1 and PMC site 2, respectively. The switches set combinatorial logic to dictate the bus speed and specific bus interface used for each PMC site as illustrated in the truth table below:

SELECTABLE PCI/PCIX BUS MODE AND SPEED CONTROL

| BUS SELECT | SPEED | PCIXCAP | 133EN | M66EN | POS 1 | POS 2 | POS 3 | POS 4 |
|---|---|---|---|---|---|---|---|---|
| PCIX | 133MHZ (DEFAULT) | 3.3V | 3.3V | D/C | OPEN | OPEN | OPEN | D/C |
| | 100MHZ | 3.3V | 0V | D/C | OPEN | OPEN | CLOSED | D/C |
| | 66MHZ | 2.48V | D/C | D/C | OPEN | CLOSED | D/C | D/C |
| PCI | 66MHZ | 0V | D/C | 3.3V | CLOSED | D/C | D/C | OPEN |
| | 33MHZ | 0V | D/C | 0V | CLOSED | D/C | D/C | CLOSED |

# 7. Performance

The XVME-9076 is designed to perform to its intended design targets, including PCI-X bus transfers at speeds up to 133MHz. Performance versus its predecessor design, the XVME-9076, is expected to be superior due to the faster PCI Express interface to the processor board and the Intel 41210 bridge device, which supports higher PCI-X speeds than were supported on the XVME-976-2X9.

Thermal performance is expected to scale with higher operational speeds at the PMC sites. The thermal solution used for the XVME-9076 requires a minimum of 200 CFM of airflow to maintain proper thermal protection of the Intel 41210 bridge device.

# 8. Top-Level Assemblies

The XVME-9076 is available in three top-level assemblies, all of which use the Xembedded XVME-9076-099 PCBA as the base assembly. The top-level assemblies are defines as follows:

| TOP-LEVEL PART | HANDLE TYPE | P0 CONNECTOR |
|---|---|---|
| XVME-9076-309 | VME-style handles | Not populated |
| XVME-9076-319 | Compact PCI-style handles | Not populated |
| XVME-9076-329 | VME-style handles | Populated |

| | | |
|---|---|---|
| XVME-9076-339 | Compact PCI-style handles | Populated |

All Top-level assemblies include PMC cover plates and shipping labels,

# 9. Product Specifications and Ratings

The XVME-9076 meets the following environmental requirements.

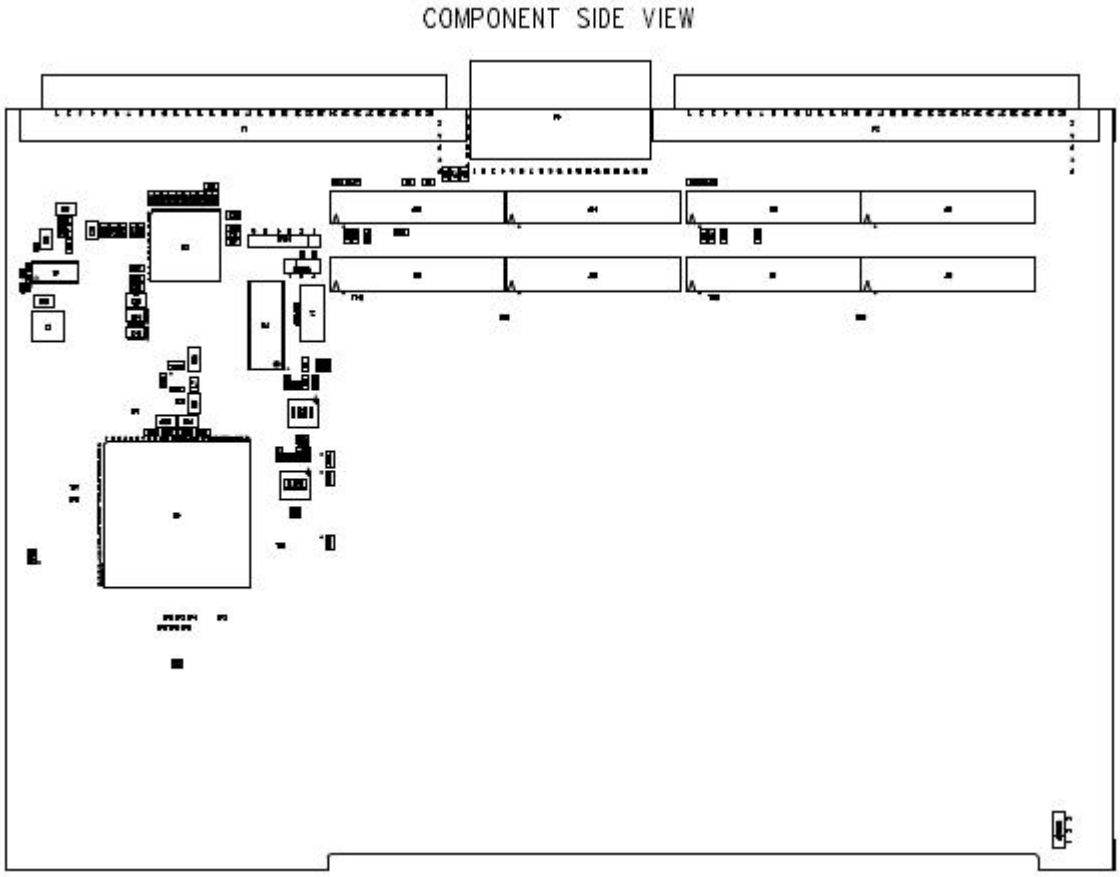
## 9.1 Environmental Specifications

The XVME-9076 is designed to meet the following environmental requirements:

| Environmental Specification | Operating | Non-Operating |
|---|---|---|
| Thermal | -20C to 70 C with 200CFM airflow | -40 to 85 C |
| Humidity | 10% to 90% RH, non-condensing | 10% to 90% RH, non-condensing |
| Shock | 30 g peak acceleration,<br>11 msec duration | 50 g peak acceleration,<br>11 msec duration |
| Vibration<br>5 – 2000 Hz | 0.015” (0.38mm) peak-to-peak displacement, 2.5 g maximum acceleration | 0.030” (0.76mm) peak-to-peak displacement, 5 g maximum acceleration |

## 9.2 Compliance Specifications / Agency Approvals

The XVME-9076 is designed to meet CE Emissions specification EN 55022 and CE Immunity specification EN 50082-2, and FCC 47 CFR, Part 15, Class A when tested in a shielded enclosure.




## 10. Power Requirements

The following power requirements include power for the Intel 41210 bridge device and the two PMC sites.

| Required voltage | Tolerances | Permissive ripple | Max. Current Requirement |
|---|---|---|---|
| +5 Volts | +0.25V / -0.125V | 50mVp-p | 12A |

Ripple and noise measurements shall be made under all specified load conditions through a single-pole low pass filter with 10 MHz cutoff frequency.